1. Preparing the inputs:

Copy the synthesized netlist, DDC and sdc output files of the synthesis run to APR/inputs area.Netlist acts as a input design for the auto place and route tool. .sdc will provide the timing information and .ddc is the complete design database.

Also copy input\_output\_delay.tcl and clock\_uncertainity.tcl into the same area.

1. Create a folder called scripts, where all the design specific .tcl files need to be created.

* Copy all the files from the zipped folder inside of scripts folder. This should include

library\_setup.tcl, read\_design.tcl, floorplan.tcl and place\_route.tcl

2(a) source the .cshrc file from your synthesis area.

1. Setting up the library (library\_setup.tcl) :

* This step will include setting up link and target libraries similar to synthesis.
* You also need to setup the techfile and the milkyway library information along with the parasicts information.
* Create a project (same name as the synthesis design name)

By sourcing the library\_setup.tcl, all these things will be done.

1. Reading the design (read\_design.tcl):

* Read the design (read output netlist from the synthesis)
* Link the libraries to this design using link command.
* Once no errors (check\_library will confirm this), you can save the design for next steps.

1. Floorplanning (floorplan.tcl):

* Create an empty core region of approximately 1.5 times that of the cell area from the synthesis report. (Currently it is set to 1.3 times)
* If there are any hard IP blocks whose area and location are fixed, be given special attention. (This is ignored as of now since we do not have any IP blocks in traffic light controller.)
* Pin locations can be preset before further proceeding the flow. (For ex. All inputs can be towards the left periphery and all the outputs can be in the right side.)
* Go through the floorplan.tcl before sourcing to understand more about these options.

1. Placement and routing:

* Here we need to provide clock and timing constraints from the input\_output\_delay.tcl and clock\_uncertainity.tcl (This includes providing the clock attributes to the clock pin).
* You can also source the \*.sdc file from synthesis output.
* Once all these steps are done, source place\_route.tcl to complete placement and routing.

1. Critical points like creating the power grid, clock grid, specifying the clock-tree synthesis and routing format have been ignored in this test case. Also information regarding running LVS, DRC and creating GDSII these will be covered the demo session.

Layout Snapshot:

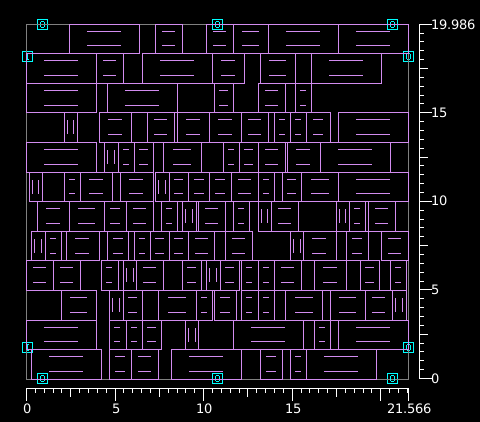
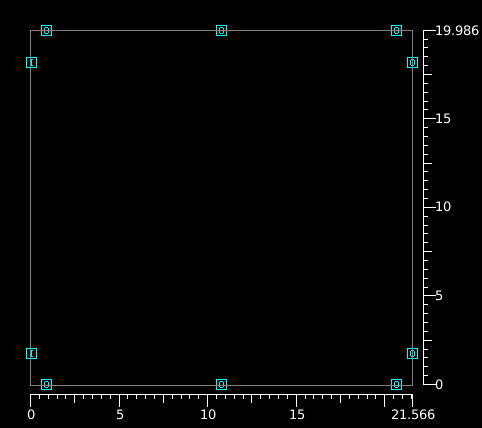


Fig. 1: Florrplan with just input, output fig. 2: Actual std.cell placed.

Pins on the periphery.

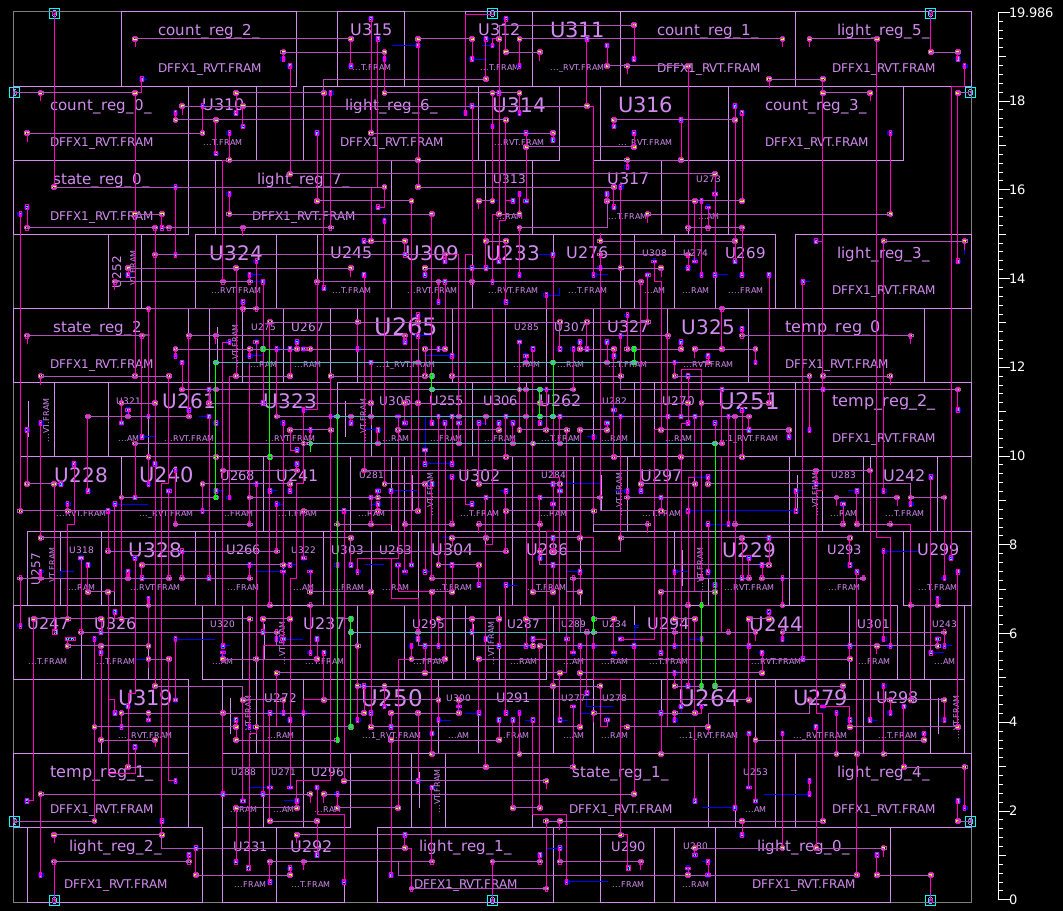
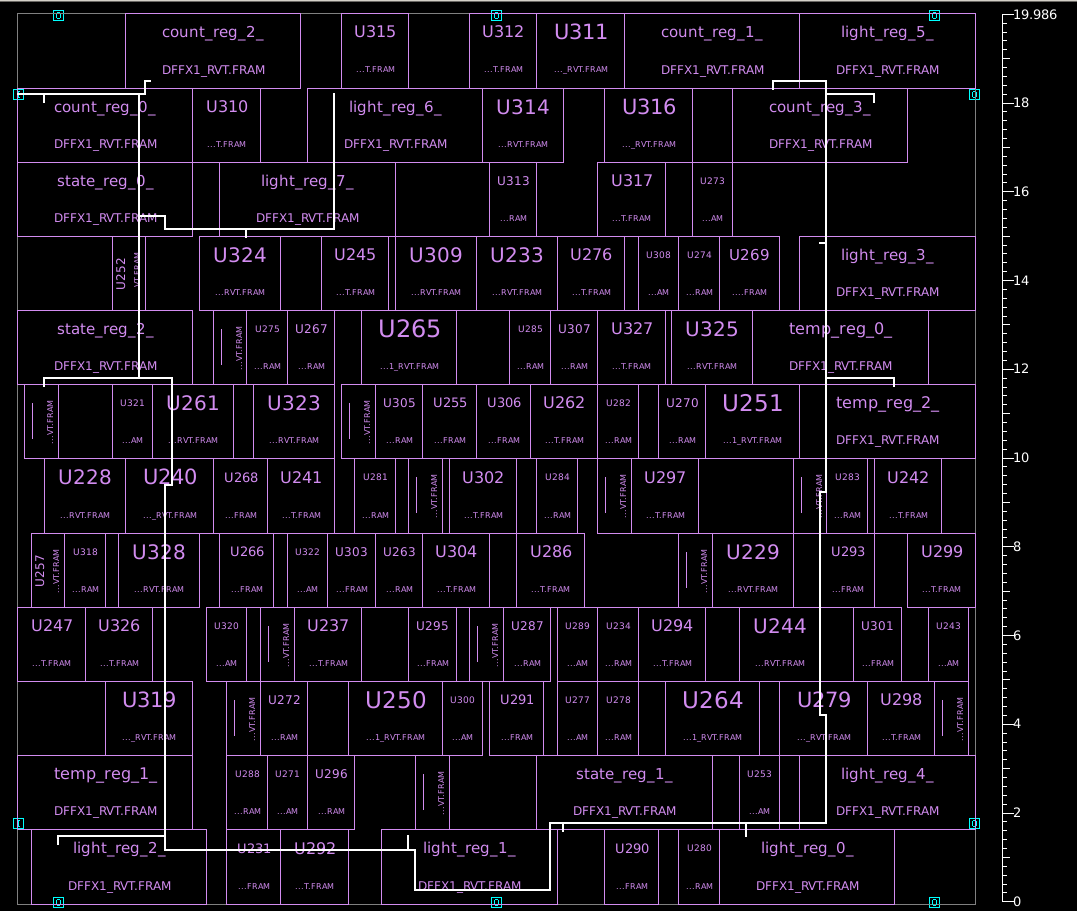


Fig. 3: Clock signal routing Fig. 4: All signals routed.

Demo files:

